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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **TAKAHASHI, Koji**

Group Art Unit: **2855**

Serial No.: **10/649,994**

Examiner: **Not yet assigned**

Filed: **August 28, 2003**

P.T.O. Confirmation No.: **6035**

For: **SEMICONDUCTOR MEMORY CAPABLE OF BEING  
DRIVEN AT LOW VOLTAGE AND ITS MANUFACTURE METHOD**

**INFORMATION DISCLOSURE STATEMENT**  
**PURSUANT TO 37 CFR 1.97(b)**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

June 17, 2004

Sir:

The attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached Form PTO-1449. One copy of each of these documents is attached, together with a copy of an Office Action in the counterpart Japanese patent application.

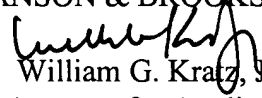
No fee or certification is required in connection with this Information Disclosure Statement, since it is being submitted prior to the issuance of a first official action on the merits or expiration of the three month period following the filing date or the entry of the national stage of the above-captioned application.

The above information is presented so that the Patent and Trademark Office can, in the first instance, determine any materiality thereof to the claimed invention. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the documents cited in the attached Form PTO-1449 be made of record therein and appear on the first page of any patent to issue therefrom.

The Commissioner is authorized to charge our Deposit Account No. 01-2340 for any fee which is deemed by the Patent and Trademark Office to be required to effect consideration of this statement.

Respectfully submitted,

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**23850**

PATENT TRADEMARK OFFICE

Enclosures: Japanese Office Action (w/translation)  
PTO-1449  
References (3)



<b>INFORMATION DISCLOSURE CITATION PTO-1449</b>	Atty. Docket No. <b>011118A</b>	Serial No. <b>10/649,994</b>
	Applicant(s): <b>TAKAHASHI, Koji</b>	
	Filing Date: <b>August 28, 2003</b>	Group Art Unit: <b>2855</b>

#### U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA					
_____	AB					
_____	AC					
_____	AD					
_____	AE					

#### FOREIGN PATENT DOCUMENTS

Document No.	Date	Country	Translation (Yes or No)
_____ AF 2000-0076792	12/26/00	Korea	No
_____ AG 2001-156188	6/08/01	Japan	Abstract only
_____ AH 05-326893	12/10/93	Japan	Abstract only
_____ AI			
_____ AJ			

#### OTHER DOCUMENTS

_____	AK	Boaz Eitan et al., NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell, IEEE ELECTRON DEVICE LETTERS, November, 2000, VOL. 21, NO. 11, PP. 543-545.
Examiner		Date Considered